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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,439	12/03/2003	Simon Lovett	2008.007100/02-0265	6743

23720 7590 09/18/2006

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EXAMINER	
WENDLER, ERIC J	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,439	LOVETT, SIMON	
	Examiner	Art Unit	
	Eric Wendler	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/7/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *updated EAST search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Amendment after Non-Final Rejection filed on June 7, 2006.

2. Claims 1-56 are pending in the present application. Claims 1, 15, 19, 30, 40, 45, 46, and 51, are independent claims.

Drawings

3. The corrected drawings were received on June 7, 2006. These drawings are accepted.

Response to Arguments

4. Applicant's arguments, see Applicant's Remarks pages 14-15, filed June 7, 2006, with respect to the 35 U.S.C. 112, first paragraph, rejection, have been fully considered and are persuasive. The rejection of claims 46-50 made under 35 U.S.C. 112, first paragraph, has been withdrawn.

5. Applicant's arguments with respect to claims 1-56 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-56, are rejected under 35 U.S.C. 102(e) as being anticipated by the US Patent to Fiscus (6,714,473), as supported by Yuh (6,154,408) and Nomura (6,304,148).

8. Regarding claims 1-2, 11, 19, 26, 30, 36, 40-41, 45-47, Fiscus teaches a memory device comprising a circuit 102 for performing an approximation of a current leakage associated with a portion of the device. Fiscus also teaches a refresh rate control unit **100,** operatively coupled with the circuit, comprising a refresh oscillator **104**, to adjust a refresh rate associated with at least a portion of the device in response to an approximation of current leakage (Fig. 1; column 1, lines 45-47; column 2, lines 31-51).

9. Regarding claims 3, 20, 31, 53, 56, Fiscus teaches the use of this circuitry with a 1T memory system. While Fiscus doesn't explicitly teach that this is a DRAM system, it is well known in the art that DRAM systems fit this description and can be used in this system as supported by Yuh (6,154,408).

10. Regarding claims 4, 15, 22, 32, 55, Fiscus teaches transistors (contained in the sense amp, Fig. 4), to provide input signals, a cell leakage model circuit 110, 112, operatively coupled to the transistor, to model a current leakage associated with a portion of the device; a comparator 130, 132, to compare the input signal to a reference input signal; and a delay unit (column 2, lines 39-43), operatively coupled to the comparator to provide a delay upon an output from the comparator to provide a time period for pre-charging of the transistor and provide a signal for controlling the refresh rate, and a refresh control oscillator 104 operatively coupled to the delay unit to provide the refresh rate signal for refreshing at least a portion of the memory device (Figs. 1,4).

11. Regarding 5-6, 23, 33, Fiscus teaches that the transistors are N-channel transistors pulled up to a supply voltage (column 4, lines 55-59). However, other types of transistors, such as P-channel transistors, can be used as they are recognized equivalents that are well known in the art. It is also well known to use both N-channel and P-channel transistors as pull-up transistors in similar systems, as taught by Nomura et al. (6,304,148).

12. Regarding claim 7, Fiscus teaches that the current leakage model comprises second transistors 150 for modeling the current leakage of at least a portion of the device.

13. Regarding claims 12, 16, 27, 37, 42, 48, Fiscus teaches that the circuit is capable of modeling a leakage current that is induced by a temperature level (column 1, lines 14-47).

14. Regarding claims 13-14, 17-18, 28-29, 38-39, 43-44, 49-50, it is inherent that operating voltage levels and particular process features induce current leakage. Whenever operating voltages or processes of memory, such as writing, are used, it is inherent that there will be induced current leakage. Fiscus teaches that his circuit is capable of modeling current leakage, which would encompass these types of inherent current leakage involved with memory.

15. Regarding claims 8-9, 24, 34, Fiscus teaches that the comparator comprises differential amplifiers 130, 132. While Fiscus doesn't explicitly teach that the comparator can be comprised of a CMOS inverter, it is well known in the art that comparators can be comprised by CMOS inverters, as supported by Yuh (6,154,408).

16. Regarding claims 19, 21, 46, 51-52, 54, while Fiscus doesn't explicitly teach a system board which is the motherboard of a computer system, a processor, a computer readable program storage device encoded with instructions that can be executed to perform a method, and a display device, which is a monitor, coupled to a computer unit with a system board, it is inherent that the system of Fiscus will require some sort of controller or processor, and these components are well-known in the art to be used as such, as supported by Yuh (6,154,408).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Irrinki et al. (5,784,328), Nomura et al. (6,304,148), and Chen Hsu et al. (6,483,764) all teach circuitry that adjusts the refresh rate of DRAM memories by using temperature or current leakage as the dependent factor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EJW
8/29/06